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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/728,772	12/08/2003	Seung-Hyun Rhee	50432-616	1077

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EXAMINER	
DAHIMENE, MAHMOUD	

ART UNIT	PAPER NUMBER
1765	

DATE MAILED: 01/04/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/728,772	RHEE ET AL.	
	Examiner	Art Unit	
	Mahmoud Dahimene	1765	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *10/31/05*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1 and 4-17* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1, 4-17* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date 12-08-03
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

Response to Arguments/Amendment

1. Applicant's arguments, filed on 10/31/2005, have been fully considered.

With respect to the rejection(s) of claims 6, 7 and 10 under 35 U.S.C. 112 second paragraph, rejection is withdrawn following applicants amendment to employ the term "poly-arylene ether".

Applicants arguments regarding that Uzoh et al. (US 6413854) and Gaw et al. (US 6303464) fail to describe or suggest the formation of caps on metal lines while a photomask is in place on the polymer ILD layer have been considered but are moot in view of the newly cited references of Wagganer (US 6146986) and Deligianni et al. (US 20050007217) because Wagganer and Deligianni provide teaching of the formation of metal lines with Uzoh's caps while a photomask is in place on the polymer ILD. A discussion of the rejection follows.

Claim Rejections - 35 USC § 103

1. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

2. Claims 1 and 4-17 are rejected under 35 U.S.C. 103(a) as being unpatentable over Uzoh et al. (US 6413854), of Gaw et al. (US 6303464) and Wagganer (US 6146986), and further in view of Deligianni et al. (US 20050007217).

Applicants are claiming a method of forming an interlevel dielectric layer, comprising the steps forming a polymer sacrificial ILD on a substrate, forming metallization structures within the polymer sacrificial ILD, etching back the polymer sacrificial ILD, non-conformally depositing dielectric material as an ILD layer over the substrate and the metallization structures so as to form air gaps in the ILD layer between at least some of the metallization structures.

Uzoh discloses a method of forming a multi-level metal (relating to applicant's claim 1) structure/ an interconnect (relating to applicant's claim 11) structure (column 9, lines 9-25). The process involves: depositing a first dielectric material (13) on a substrate (11) (column 9, line 11) (figures 5-13), patterning the first dielectric material (column 9, line 12) (figure 6); depositing at least one metal (19) in openings in the patterned first dielectric and on the patterned first dielectric material, removing portions of the at least one metal at least in a region above an upper surface of the first dielectric material (column 9, lines 16-19) (figures 8-9), removing the first dielectric material (column 9, line 20) (figure 12), and providing a second dielectric material (43) in place of the first dielectric material (column 9, line 21) (figure 13).

A difference is noted between applicant's claims and the reference of Uzoh. Uzoh fails to teach a step corresponding to the applicant's step consisting of depositing the metal lines and cap layer while the photomask is on the IDL layer.

Wagganer teaches a lithographic method for creating damascene metallization layers wherein the method of performing the lithographic damascene etch comprises the steps of depositing a photoresist layer (316) above the layer stack and forming a trench in the photoresist layer so that the trench is positioned over the underlying layer of the layer stack. The method continues with depositing a metal layer over the top surface of the photoresist layer and filling the trench with the metal (such as copper) (column 3, line 40) and (column 5, line 60). The method of Wagganer involves filling the said trench to the top and following with a planarization step, however, Deligianni teaches a similar method wherein the deposited metal (110) is partially filling the trench (figures 6a-6c), therefore, not necessitating a planarization step before removal of the photomask (PR) (72) (page 4, paragraph 32). The step of deposition of a metal cap layer while the photomask is on the polymer sacrificial layer is not disclosed by Wagganer or Deligianni, Wagganer discusses an optional dielectric cap layer on the last metallization layer, however, one of ordinary skill in the art would have been motivated to deposit the metallic Ta cap layer (disclosed by Uzoh (column 4, line 65)) before the removal of the photoresist photomask because Uzoh cites it is conventional to cap the copper lines with Ta, deposition of a Ta layer after removal of the photoresist, in the method of Wagganer would cause electrical short-circuits between metal line, so deposition of the cap Ta layer would be more obvious immediately after copper deposition before removing the photomask layer.

A second difference is noted between applicant's claims and the reference of Uzoh. Uzoh fails to teach a step corresponding to the applicant's step consisting of depositing a non-conformal dielectric material in claim 1.

Gaw teaches a similar semiconductor manufacturing process for reducing the interconnect system capacitance through enclosed voids in a dielectric layer. See abstract. Gaw discloses that after removal of the first dielectric, which could be a Fluoropolymer, deposition of a non-conformal dielectric over the substrate on a metal layer, and on the trenches between interconnects such that voids or air gaps are formed, is desirable because air voids between interconnects lower the effective dielectric constant between metal lines, reducing capacitance, and cross-talk effects (column 1, lines 14-34).

Therefore, it would have been obvious to one of ordinary skill in the art at the time of the invention was made to modify the process of Uzoh to deposit metal and cap layers while the photomask (photoresist) is still on the sacrificial ILD layer and to include the step of depositing a non-conformal dielectric layer allowing the formation of air gaps in the second dielectric between metal lines because the combined references of Wagganer and of Deligianni teach that it is conventional to deposit metal over a patterned photoresist layer to fill trenches in order to lower damage risks associated with chemical mechanical polishing (Wagganer; Column 2, line 56), the photomask is removed after metal (and cap) deposition as cited by Deligianni, as to lowering the dielectric k-value, Gaw illustrates that introducing air gaps between metal lines is

desirable because it results in the production of a chip with less capacitance delay and interconnect cross-talk.

One of ordinary skill in the art would have been motivated to deposit metal and cap layers over pattern photoresist because the reference of Wagganer discloses the improved lithographic damascene techniques have many inherent advantages which solves many of the problems encountered with earlier methods that relate to profile control and material properties, for example, metal etchability and the porosity and mechanical strength of the dielectric materials (column 8, line 50), and to include air gaps in the second dielectric in order to obtain less capacitance and cross-talk effects resulting in the capability of manufacturing a faster chip (Gaw; column 1, lines 14 to column 2, line 32).

As to claim 4, Uzoh discloses that the cap layer on top of the copper may protect the metal during the first dielectric etch (column 5, line 24).

As to claim 5, Uzoh includes Ta as a cap layer (column 4, line 65).

As to claim 6, Uzoh includes SilK (poly-arylene ether) as a first dielectric material (column 3, line 39).

As to claim 7, Uzoh does not explicitly disclose using SiO_2 / SiOF as materials for the ILD layer, Gaw discloses SiO_2 or SiOF as materials for the ILD layer (column 4, line 20).

The characteristics of SiO_2 materials for non-conformal deposition are well known in the art (Wolf et al. (Volume1, page 183)), allowing for a reliable method to include voids (or air gaps). Also, SiOF has a lower k value (Wolf et al. (Volume 4, page 654))

and similar mechanical properties as SiO_2 consequently it is also desirable for applications that require low-k dielectrics.

Therefore, it would have been obvious to one of ordinary skill in the art at the time of the invention was made to modify the process of Uzoh by selecting SiO_2 or SiOF as a second ILD because Gaw discloses a method for reducing capacitance and cross-talk effects between metal interconnect lines by including voids or air gaps by using SiO_2 or SiOF. One of ordinary skill in the art would have been motivated to include SiO_2 or SiOF materials as the second dielectric because the use of these materials allows formation of air gaps which in turns lowers the k value between metal lines.

As to claims 8, 9 and 16, Uzoh discloses a method, wherein, a mask is not needed to etch back the sacrificial ILD layer (which could be a polymer), (column 9, lines 9-24), making it a self-aligned process.

As to claims 10 and 14, both Uzoh and Gaw include the possibility of using any dielectric material having a low dielectric constant (Uzoh, column 8, line 5) such as porous silica, etc.

Therefore, it would have been obvious to one of ordinary skill in the art at the time of the invention was made to modify the process of Uzoh to include any ultra low k dielectric (provided the material meets all manufacturing and reliability requirements) as a second ILD, as taught by Gaw (column 1, line 45) because it is desirable to lower the dielectric k value between metal lines to reduce capacitance and cross-talk effects. One of ordinary skill in the art would have been motivated to include ultra low k materials as the second dielectric in order to obtain a faster chip (Wolf et al. (Volume 4, page 663).

As to claim 12, Uzoh fails to disclose a second dielectric layer comprising voids (or air gaps) between consecutive metal lines, however, Gaw discloses a second dielectric layer non-conformally deposited over the metal lines forming voids (air gaps) between the metal lines (column 10, line 21).

Therefore, it would have been obvious to one of ordinary skill in the art at the time of the invention was made to modify the process of Uzoh to include air gaps in the second dielectric because Gaw illustrates that introducing air gaps is desirable because it results in the production of a chip with less capacitance delay and interconnect cross-talk. One of ordinary skill in the art would have been motivated to include air gaps in the second dielectric in order to obtain a faster chip.

As to claims 13, 15 and 17, Uzoh includes copper as a typical fill for copper lines (column 4, line 44), and Tantalum as a cap layer (column 4, line 65).

The present rejection addresses applicants arguments related to the method comprising the steps of forming a polymer sacrificial ILD on a substrate and a photomask on the polymer sacrificial ILD. Recesses are etched in the polymer sacrificial ILD through the photomask. Metalization structures are formed within the polymer sacrificial ILD while the photomask is on the polymer sacrificial ILD because the reference of Wagganer teaches a method of depositing metal (copper) over a patterned photoresist layer, and the reference of Deligianni teaches a method where the metal deposition, in the photoresist openings, does not fill the entire openings and therefor planarization of the metal is not needed, it would be obvious to one of ordinary skill in

the art to use the combined teachings of Wagganer and Deligianni applied to the method of Uzoh to deposit the metal in the patterned sacrificial ILD while the photoresist is on the sacrificial ILD stopping the deposition at the ILD surface level because Wagganer discloses the improved lithographic damascene techniques have many inherent advantages which solves many of the problems encountered with earlier methods that relate to profile control and material properties, for example, metal etchability and the porosity and mechanical strength of the dielectric materials (column 8, line 50). As to the deposition of a metal cap layer on the copper deposited within the recesses while the photomask is on the ILD sacrificial layer, Uzoh discloses a metal cap layer to protect the metal top surface, but none of the references cited disclose deposition of the cap layer while the photomask is on the ILD sacrificial layer, however, one of ordinary skill in the art would have been motivated to deposit the metallic Ta cap layer (disclosed by Uzoh (column 4, line 65)) before the removal of the photoresist photomask because Uzoh cites it is conventional to cap the copper lines with Ta, deposition of a Ta layer after removal of the photoresist, in the method of Wagganer would cause electrical short-circuits between metal line, so deposition of the cap Ta layer would be more obvious immediately after copper deposition before removing the photomask layer.

Conclusion

3. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP

§ 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

4. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Mahmoud Dahimene whose telephone number is (571) 272-2410. The examiner can normally be reached on week days from 8:00 AM. to 5:00 PM..

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Nadine Norton can be reached on (571) 272-1465. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

LAN VINH
PRIMARY EXAMINER

Mohammad Dahimene
MD